REMARKS

This is a full and timely response to the outstanding non-final Office Action mailed April 1, 2009. Claims 24-26, 29-35, and 38-43 are pending. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

Rejections under 35 U.S.C. § 112

The Office Action indicates that claim 43 stands rejected as allegedly failing to comply with the written description requirement. The Office Action alleges that "a decoder, coupled to the control circuit, for receiving a first number of outputs from the control circuit and thereby generating a second number of outputs; wherein the second number is larger than the first number," as recited in claim 43, is "not supported in the original specification nor in any claims original filed." Applicant traverses the rejection.

In the "Response to Arguments" section, the Office Action (pp. 11-12) alleges that support for "generating a second number of outputs; wherein the second number is larger than the first number" was not found. The Office Action also alleged that "the definition of the first number and the second number" was not found. As stated in Applicant's last response, the specification at page 5, lines 17-21, supports this claim feature:

> The output signal of the controlling device 11 can first feed into a decoding device 12, and then couple to the detecting device 13 and the multiplexer 16, in order to reduce the number of outputs of the controlling device 11. As shown in Fig. 2B, the decoding device 12 can be a 3 to 8 decoder (3x8 decoder).

This portion clearly discloses that a decoding device can be a 3 to 8 decoder; *i.e.*,

having three inputs and eight outputs. The second number (8) is larger than the first number (3). The decoding device (decoder) is coupled to a controlling device (control circuit). The stated purpose is to reduce the number of outputs of the controlling device, which, in the example, needs only three outputs instead of eight. An example of such a decoding device is presented in FIG. 2B. Applicant also notes that a similar feature is recited in claim 32, which is not subject to this rejection. Accordingly, Applicant submits that the rejection is improper and should be withdrawn.

Rejections under 35 U.S.C. § 103

The Office Action indicates that claims 24-26, 29-33, and 35 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over *Patterson et al.* (US Pub. 2004/0081099, hereinafter *Patterson*). Applicant traverses the rejection. In order for a claim to be properly rejected under 35 U.S.C. § 103, the teachings of the prior art reference must suggest all features of the claimed invention to one of ordinary skill in the art. *See, e.g., In re Dow Chemical*, 837 F.2d 469, 5 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1988); *In re Keller*, 642 F.2d 413, 208 U.S.P.Q. 871, 881 (C.C.P.A. 1981).

To begin, independent claim 24 recites:

> 24. An apparatus for automatically determining a type of an external device, comprising:
> a jack for coupling the external device;
> ***an impedance detecting circuit, coupled to the external device through the jack, for generating a first analog signal according to an impedance of the external device and a first resistance, a second analog signal according to the impedance of the external device and a second resistance and a third analog signal according to the impedance of the external device and a third resistance, wherein the first, second and third resistances are different***;
> ***an analog-to-digital converter, coupled to the impedance detecting circuit, for converting the first, second and third analog signals to first, second and third digital values, respectively***; and

> ***a control circuit, coupled to the analog-to-digital converter, for determining the type of the external device when the first digital value falls within a first predetermined range, the second digital value falls within a second predetermined range, the third digital value falls within a third predetermined range and all of the first, second and third predetermined ranges together indicate a same recognized condition among a plurality of predetermined recognized conditions***;
>
> ***wherein the impedance detecting circuit comprises a plurality of resistors, which couples together in parallel, for providing the first, second and third resistance and each of the first, second and third digital values is a multi-bit number***.

(*Emphasis added*). Applicant respectfully submits that *Patterson* fails to disclose, teach, or suggest at least the features emphasized above in claim 24.

As a preliminary matter, Applicant objects to the manner in which the Examiner has rejected Applicant's claims. In particular, Applicant notes that, as before during prosecution of the instant patent application, the Examiner has simply block copied Applicant's claim limitations and provided citations to features from drawings of the reference *without any explanation whatsoever* as to how those features either teach Applicant's explicit limitations or render those limitations obvious. Again, the Supreme Court has explicitly stated that the Examiner must provide "some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *KSR v. Teleflex*, 127 S. Ct. 1727, 1741, 82 U.S.P.Q.2d at 1396 (quoting *In re Kahn*, 441 F.3d 977, 988, 78 U.S.P.Q.2d 1329, 1336 (Fed. Cir. 2006)). Clearly, the Examiner has provided no such reasoning.

Because of the Examiner's failure to explain how those drawing elements disclose or suggest Applicant's claim language, Applicant was, and is still, left to guess as to why the Examiner believes that the various drawing elements cited by the Examiner teach or suggest Applicant's claim language. In view of that fact, Applicant

has been denied a full opportunity to understand the reasons why Applicant's claims have been rejected and, therefore, has likewise been denied an opportunity to properly respond to the rejections. In other words, Applicant's case has been unfairly prejudiced by the Examiner's actions.

It is stated in MPEP § 706.07 that "[t]he Examiner should never lose sight of the fact that in every case the applicant is entitled to a full and fair hearing, and that a clear issue between applicant and examiner should be developed, if possible, before appeal." In this case, no "clear issue" was ever developed by the Examiner. In view of the Examiner's actions, Applicant submits that the Examiner issue a further *non-final* Office Action that provides the explanations that had been omitted by the Examiner, or allow all claims.

Regarding the impedance detection circuit, the Office Action (p. 3) alleges that R1, R5, and R6 of FIG. 9B correspond to the first, second, and third resistances, respectively. Applicant notes that the Office Action has not identified features of *Patterson* that allegedly correspond to first, second, and third analog signals that are generated according to the impedance of the external device and the respective resistance. Instead, the Office Action has merely pointed out three different resistors from the reconfiguration circuit 32e.

Applicant again submits that the reconfiguration circuit 32e has a different function from an "impedance detection circuit" as recited in this feature of claim 24. The reconfiguration circuit "responds to the identification of a particular load at a particular jack by load sensing circuit 30 and reconfigures the circuits associated with that connector so that they are properly adapted for the identified load." ([0045]). Nowhere

does *Patterson* disclose, teach, or suggest generating three analog signals in the reconfiguration circuit according to the impedance of the external device concurrently with three different resistances. Furthermore, this Office Action points to resistor R5, which is part of a "programmable microphone bias source controlled by the level on input 260." ([0060]). Thus, even assuming, *arguendo*, that a signal is generated according to R5, the signal is not generated according to the impedance of the external device.

Regarding the analog to digital converter, the Office Action (p. 4) alleges that FIG. 4 at 34 and 36 and page 4 at [0049] of *Patterson* corresponds to this feature. Applicant notes that no analog to digital converter is shown within block 34 in FIG. 4. Paragraph [0049] of *Patterson* states in pertinent part: "Response analyzer 36 includes analog to digital converter 124, preferably a programmable amplifier and sample and hold circuit 126 along with switches 128 and 130. Identification circuit 38 includes data analysis logic circuit 132." The Office Action fails to identify where *Patterson* allegedly teaches that either of the analog-to-digital converters is "for converting the first, second and third analog signals to first, second and third digital values, respectively" as recited in claim 24.

Applicant notes that the analog to digital converter 124 in the response analyzer 36 is in a different circuit from where the Office Action alleged that the resistances for generating the first, second, and third analog signals were located. Further, the analog to digital converter 124 appears to digitize just one signal, instead of three analog signals generated by an impedance detection circuit using the impedance of the external device and three different resistances. ("[A]gain the signal is converted to

digital form by ADC converter 124 and delivered to data analysis logic circuit 132," *Patterson* at [0050]). ADC1 is within the reconfiguration circuit 32, but it appears to merely digitize one analog audio signal, not three analog signals generated by an impedance detection circuit using the impedance of the external device and three different resistances. ("Amplifier 92 would buffer the incoming signal for further processing such as digitizing by an audio ADC," *Patterson* at [0052]).

Regarding the control circuit, the Office Action (p. 4) alleges that elements 146, 150, and 154 of FIG. 5 correspond to three digital values falling within a respective predetermined range. However, all three of the blocks on FIG. 5 are using the same "tip" signal, not three digital values. The "tip" signal is not generated according to three analog signals respectively associated with three different resistances as recited in the claim. (*See* FIGS. 4-5 and paragraphs [0048]-[0050] of *Patterson*).

Regarding the wherein clause, the Office Action (p. 4) takes a different point of view to allege that numbers JS0, JS1, and JS3 of FIGS. 9A, 9B and 10 correspond to the three digital values. However, *Patterson* teaches that the decision tree of FIG. 5 is carried out by the circuit of FIG. 4, while the jack sensing table of FIG. 10 is carried out by the circuits of FIGS. 9A and 9B. Since the circuit of FIG. 4 is completely different from the circuits of FIGS. 9A and 9B, a person of ordinary skill in the art will recognize that the decision tree of FIG. 5 is completely different from the jack sensing table of FIG. 10 in function and structure. Even assuming, *arguendo*, that the decision tree is equivalent to the jack sensing table, the numbers JS0, JS1 and JS3 is generated by comparing an input V1 with an input V2, not generated according to three analog signals generated by an impedance detection circuit of using the impedance of the

external device and three different resistances as taught in claim 24. (*See* FIGS. 9A, 9B and 10 and paragraphs [0059] of *Patterson*). Moreover, each of the numbers JS0, JS1, and JS3 is a single-bit number instead of a multi-bit number as required in claim 24.

For at least these reasons, Applicant respectfully submits that claim 24 is allowable and respectfully request that the rejection be withdrawn. Insofar as claims 25-26 and 29-32 depend from claim 24, claims 25-26 and 29-32 are allowable as a matter of law because these dependent claims contain all features/elements/steps of their independent claim. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988). Therefore, Applicant respectfully requests that the rejection of claims 25-26 and 29-32 be withdrawn.

Next, independent claim 33 recites:

> A method for automatically determining a type of an external device, comprising:
> providing a plurality of predetermined resistances by a plurality of resistors coupled together in parallel;
> ***generating a first analog signal according to a first coupling relation between a the plurality of predetermined resistances and an impedance of the external device;***
> ***generating a second analog signal according to a second coupling relation, which is different from the first coupling relation, between the plurality of predetermined resistances and the impedance of the external device;***
> ***generating a third analog signal according to a third coupling relation, which is different from the first and second coupling relations, between the plurality of predetermined resistances and the impedance of the external device;***
> ***respectively converting the first, second and third analog signals to first, second and third digital values***; and
> ***determining the type of the external device when the first digital value falls within a first predetermined range, the second digital value falls within a second predetermined range, the third digital value falls within a third predetermined range and all of the***

first, second and third ranges together indicate a same recognized condition among a plurality of predetermined recognized conditions;
wherein each of the first, second and third digital values is a multi-bit number.

(*Emphasis added*). Applicant respectfully submits that *Patterson* fails to disclose, teach, or suggest at least the features emphasized above in claim 33.

Regarding the first, second, and third analog signals, the Office Action (p. 6) alleges that R1, R5, and R6 of FIG. 9B correspond to these signals, respectively. Applicant notes that the Office Action has not identified features of *Patterson* that allegedly correspond to first, second, and third analog signals that are generated according to different coupling relations "between the plurality of predetermined resistances and the impedance of the external device." Instead, the Office Action has merely pointed out three different resistors from the reconfiguration circuit 32e.

Applicant submits that nowhere does *Patterson* disclose, teach, or suggest generating three analog signals in the reconfiguration circuit according to different coupling relations "between the plurality of predetermined resistances and the impedance of the external device." Furthermore, this Office Action points to resistor R5, which is part of a "programmable microphone bias source controlled by the level on input 260." ([0060]). Thus, even assuming, *arguendo*, that a signal is generated according to R5, the signal is not generated according to a coupling relation "between the plurality of predetermined resistances and the impedance of the external device."

Regarding converting analog signals to digital values, the Office Action (p. 6) alleges that FIG. 4 at 34 and 36 and page 4 at [0049] of *Patterson* corresponds to this feature. Applicant notes that no analog to digital converter is shown within block 34 in FIG. 4. Paragraph [0049] of *Patterson* states in pertinent part: "Response analyzer 36

includes analog to digital converter 124, preferably a programmable amplifier and sample and hold circuit 126 along with switches 128 and 130. Identification circuit 38 includes data analysis logic circuit 132." The Office Action fails to identify where *Patterson* allegedly teaches that either of the analog-to-digital converters is "for converting the first, second and third analog signals to first, second and third digital values, respectively" as recited in claim 24.

Applicant notes that the analog to digital converter 124 in the response analyzer 36 is in a different circuit from where the Office Action alleged that the resistances for generating the first, second, and third analog signals were located. Further, the analog to digital converter 124 appears to digitize just one signal, instead of three analog signals generated by an impedance detection circuit using the impedance of the external device and three different resistances. ("[A]gain the signal is converted to digital form by ADC converter 124 and delivered to data analysis logic circuit 132," *Patterson* at [0050]). ADC1 is within the reconfiguration circuit 32, but it appears to merely digitize one analog audio signal, not three analog signals generated by an impedance detection circuit using the impedance of the external device and three different resistances. ("Amplifier 92 would buffer the incoming signal for further processing such as digitizing by an audio ADC," *Patterson* at [0052]).

Regarding determining the type of the external device, the Office Action (p. 6) alleges that elements 146, 150, and 154 of FIG. 5 correspond to three digital values falling within a respective predetermined range. However, all three of the blocks on FIG. 5 are using the same "tip" signal, not three digital values. The "tip" signal is not generated according to three analog signals respectively associated with three different

resistances as recited in the claim. (*See* FIGS. 4-5 and paragraphs [0048]-[0050] of *Patterson*).

Regarding the wherein clause, the Office Action (p. 7) takes a different point of view to allege that numbers JS0, JS1, and JS3 of FIGS. 9A, 9B and 10 correspond to the three digital values. However, *Patterson* teaches that the decision tree of FIG. 5 is carried out by the circuit of FIG. 4, while the jack sensing table of FIG. 10 is carried out by the circuits of FIGS. 9A and 9B. Since the circuit of FIG. 4 is completely different from the circuits of FIGS. 9A and 9B, a person of ordinary skill in the art will recognize that the decision tree of FIG. 5 is completely different from the jack sensing table of FIG. 10 in function and structure. Even assuming, *arguendo*, that the decision tree is equivalent to the jack sensing table, the numbers JS0, JS1 and JS3 is generated by comparing an input V1 with an input V2, not generated according to three analog signals generated by an impedance detection circuit of using the impedance of the external device and three different resistances as taught in claim 33. (*See* FIGS. 9A, 9B and 10 and paragraphs [0059] of *Patterson*). Moreover, each of the numbers JS0, JS1, and JS3 is a single-bit number instead of a multi-bit number as required in claim 33.

For at least these reasons, Applicant respectfully submits that claim 33 is allowable and respectfully request that the rejection be withdrawn. Insofar as claim 35 depends from claim 33, claim 35 is allowable as a matter of law because it contains all features/elements/steps of its independent claim. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988). Therefore, Applicant respectfully requests that the rejection of claim 35 be withdrawn.

The Office Action indicates that claims 34 and 38-43 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over *Patterson* in view of *Dao* (US 6,407,633). Applicant traverses the rejection.

Regarding claim 34, Applicant respectfully submits that the addition of *Dao* fails to cure the deficiencies of *Patterson* discussed in connection with independent claim 33. Moreover, Applicant respectfully disagrees with the alleged motivation for combining *Dao* with *Patterson*, "to provide better sound quality for each channel." (Office Action, p. 8). The Office Action has not provided any reasoning to support such a conclusion. Again, the Supreme Court has explicitly stated that the Examiner must provide "some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *KSR v. Teleflex*, 127 S. Ct. 1727, 1741, 82 U.S.P.Q.2d at 1396 (quoting *In re Kahn,* 441 F.3d 977, 988, 78 U.S.P.Q.2d 1329, 1336 (Fed. Cir. 2006)). Insofar as claim 34 depends from claim 33, claim 34 is allowable as a matter of law because it contains all features/elements/steps of its independent claim. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988). Therefore, Applicant respectfully requests that the rejection of claim 34 be withdrawn.

Next, independent claim 38 recites:

> 38. An apparatus for determining a type of an external device, comprising:
> a jack for coupling the external device;
> ***an impedance detecting circuit, coupled to the external device through the jack, for generating a first analog signal according to an impedance of the external device and a first resistance, a second analog signal according to the impedance of the external device and a second resistance and a third analog signal according to the impedance of the external device and a third resistance***, the impedance detecting circuit comprising:

a plurality of detecting paths coupled together in parallel, ***each of the detecting paths comprising a resistor and a transistor coupled together in series, and on/off conditions of the transistors determining the first, second and third resistances***;

an analog-to-digital converter, coupled to the impedance detecting circuit, for converting the first, second and third analog signals to first, second and third digital values; and

a control circuit, coupled to the analog-to-digital converter, for determining the type of the external device when the first digital value falls within a first predetermined range, the second digital value falls within a second predetermined range, the third digital value falls within a third predetermined range and all of the first, second and third predetermined ranges together indicate a recognized condition among a plurality of predetermined recognized conditions;

wherein the first, second and third resistances are different and each of the first, second and third digital values is a multi-bit number.

(*Emphasis added*). Applicant respectfully submits that the cited references to disclose, teach, or suggest at least the features emphasized above in claim 38.

Regarding the impedance detection circuit, the Office Action (p. 8) alleges that R1, R5, and R6 of FIG. 9B in *Patterson* correspond to the first, second, and third resistances, respectively. Applicant notes that the Office Action has not identified features of *Patterson* that allegedly correspond to first, second, and third analog signals that are generated according to the impedance of the external device and the respective resistance. Instead, the Office Action has merely pointed out three different resistors from the reconfiguration circuit 32e.

Applicant again submits that the reconfiguration circuit 32e has a different function from an "impedance detection circuit" as recited in this feature of claim 24. The reconfiguration circuit "responds to the identification of a particular load at a particular jack by load sensing circuit 30 and reconfigures the circuits associated with that connector so that they are properly adapted for the identified load." ([0045]). Nowhere

does *Patterson* disclose, teach, or suggest generating three analog signals in the reconfiguration circuit according to the impedance of the external device. Furthermore, this Office Action points to resistor R5, which is part of a "programmable microphone bias source controlled by the level on input 260." ([0060]). Thus, even assuming, *arguendo*, that a signal is generated according to R5, the signal is not generated according to the impedance of the external device.

Regarding the analog to digital converter, the Office Action (p. 9) alleges that FIG. 4 at 34 and 36 and page 4 at [0049] of *Patterson* corresponds to this feature. Applicant notes that no analog to digital converter is shown within block 34 in FIG. 4. Paragraph [0049] of *Patterson* states in pertinent part: "Response analyzer 36 includes analog to digital converter 124, preferably a programmable amplifier and sample and hold circuit 126 along with switches 128 and 130. Identification circuit 38 includes data analysis logic circuit 132." The Office Action fails to identify where *Patterson* allegedly teaches that either of the analog-to-digital converters is "for converting the first, second and third analog signals to first, second and third digital values, respectively" as recited in claim 24.

Applicant notes that the analog to digital converter 124 in the response analyzer 36 is in a different circuit from where the Office Action alleged that the resistances for generating the first, second, and third analog signals were located. Further, the analog to digital converter 124 appears to digitize just one signal, instead of three analog signals generated by an impedance detection circuit using the impedance of the external device and three different resistances. ("[A]gain the signal is converted to digital form by ADC converter 124 and delivered to data analysis logic circuit 132,"

Patterson at [0050]). ADC1 is within the reconfiguration circuit 32, but it appears to merely digitize one analog audio signal, not three analog signals generated by an impedance detection circuit using the impedance of the external device and three different resistances. ("Amplifier 92 would buffer the incoming signal for further processing such as digitizing by an audio ADC," *Patterson* at [0052]).

Regarding the control circuit, the Office Action (p. 9) alleges that elements 146, 150, and 154 of FIG. 5 correspond to three digital values falling within a respective predetermined range. However, all three of the blocks on FIG. 5 are using the same "tip" signal, not three digital values. The "tip" signal is not generated according to three analog signals respectively associated with three different resistances as recited in the claim. (*See* FIGS. 4-5 and paragraphs [0048]-[0050] of *Patterson*).

Regarding the wherein clause, the Office Action (p. 9) takes a different point of view to allege that numbers JS0, JS1, and JS3 of FIGS. 9A, 9B and 10 correspond to the three digital values. However, *Patterson* teaches that the decision tree of FIG. 5 is carried out by the circuit of FIG. 4, while the jack sensing table of FIG. 10 is carried out by the circuits of FIGS. 9A and 9B. Since the circuit of FIG. 4 is completely different from the circuits of FIGS. 9A and 9B, a person of ordinary skill in the art will recognize that the decision tree of FIG. 5 is completely different from the jack sensing table of FIG. 10 in function and structure. Even assuming, *arguendo*, that the decision tree is equivalent to the jack sensing table, the numbers JS0, JS1 and JS3 is generated by comparing an input V1 with an input V2, not generated according to three analog signals generated by an impedance detection circuit of using the impedance of the external device and three different resistances as taught in claim 38. (*See* FIGS. 9A, 9B

and 10 and paragraphs [0059] of *Patterson*). Moreover, each of the numbers JS0, JS1, and JS3 is a single-bit number instead of a multi-bit number as required in claim 38.

Applicant respectfully submits that the addition of *Dao* fails to cure the deficiencies of *Patterson* discussed above. Further, the Office Action (p. 9) admits that "Patterson does not explicitly teach each of the detecting paths comprising a resistor and transistor coupled together in series, and on/off conditions of the transistors determining the first, second, and third resistances." The Office Action (p. 10) alleges that *Dao* teaches this feature and that "it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Dao into the teaching of Patterson to provide better sound quality for each channel." Applicant respectfully disagrees. The Office Action has not provided any reasoning to support the conclusion that *Dao* would "provide better sound quality for each channel." Again, the Supreme Court has explicitly stated that the Examiner must provide "some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *KSR v. Teleflex*, 127 S. Ct. 1727, 1741, 82 U.S.P.Q.2d at 1396 (quoting *In re Kahn,* 441 F.3d 977, 988, 78 U.S.P.Q.2d 1329, 1336 (Fed. Cir. 2006)). Further, as shown in FIG. 9B of *Patterson*, the purported resistances are all related to the left channel and not the right channel. Therefore, the combination of *Patterson* in view of *Dao* would be nonsensical and would not improve the sound quality for ***each channel***.

For at least these reasons, Applicant respectfully submits that claim 38 is allowable and respectfully request that the rejection be withdrawn. Insofar as claims 39-43 depend from claim 38, claims 39-43 are allowable as a matter of law because these dependent claims contain all features/elements/steps of their independent claim. *In re*

Fine, 837 F.2d 1071, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988). Therefore, Applicant respectfully requests that the rejection of claims 39-43 be withdrawn.

It is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

No fee is believed to be due in connection with this submission. If, however, any fee is deemed to be payable, you are hereby authorized to charge any such fee to Deposit Account No. 20-0778.

Respectfully submitted,

/Daniel R. McClure/

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